REMARKS

Claims 1-26 were pending in this application.

Claims 1-26 have been rejected.

No claims have been allowed.

No claims have been amended.

Claims 1-26 remain in this case. A copy of all pending claims is provided below in the Appendix for the convenience of the Examiner.

Reconsideration and full allowance of Claims 1-26 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-26 as being unpatentable over U.S. Patent No. 5,394,524 to DiNicola et al. ("*DiNicola*") in view of U.S. Patent No. 6,208,350 to Herrera ("*Herrera*"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d

1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

The Office Action fails to establish that the proposed *DiNicola-Herrera* combination discloses, teaches, or suggests "dual mode sub-processing circuitry" that is operable to perform "motion compensation operations" associated with a two-dimensional image pipeline in one mode and to perform "rasterization operations" associated with a three-dimensional image pipeline in another mode.

DiNicola recites a graphics system that processes 2D and 3D data streams concurrently. (*Abstract*). The system includes a reordering device (element 322), which receives 2D data from a 2D subsystem and 3D data from a 3D subsystem. (*Col. 2, Lines 23-35*). The reordering device then provides the 2D and 3D data to a raster subsystem (element 326), which processes the data. (*Col. 2, Lines 13-35*).

As acknowledged in the Office Action, *DiNicola* contains no mention of performing "motion compensation operations." (*Office Action, Page 3, First paragraph*). Moreover, while *DiNicola* recites the performance of raster operations by the raster subsystem, *DiNicola* contains no mention that the raster subsystem performs the raster operations while in one of multiple "modes." Instead, the raster subsystem always performs raster operations no matter what type of data it is processing.

The Office Action asserts that an "attribute processor" of *DiNicola* is the equivalent of the "dual mode sub-processing circuitry" recited in Claim 1. (*Office Action, Page 2, Last paragraph*). However, the attribute processor in *DiNicola* pre-processes data before the data is provided to the 2D and 3D subsystems. (*Col. 5, Lines 55-61*). The attribute processor of *DiNicola* does not perform "motion compensation operations" or "raster operations." As a result, the attribute processor of *DiNicola* cannot anticipate the "dual mode sub-processing circuitry" recited in Claim 1.

Herrera recites a 3D graphics accelerator modified to support MPEG-2 video decoding. (*Abstract*). A graphics engine generates digital image data based on at least one command signal from a processor. (*Col. 5, Lines 53-57*). The graphics engine also generates motion compensated

digital image data based on at least one digital image and at least one motion vector. (*Col. 5, Lines 57-58*).

Herrera recites the generation of digital image data and "motion compensated" digital image data by a graphics engine. The Office Action fails to establish that the "motion compensated" digital image data is generated by "dual mode" circuitry operating in one of multiple "modes" as recited in Claim 1.

The Office Action relies on the graphics engine and the command signal of *Herrera* as anticipating these elements of Claim 1. However, the command signal of *Herrera* invokes the generation of the digital image data by the graphics engine. The Office Action fails to show how the command signal of *Herrera* invokes "motion compensation operations" in one mode and "rasterization operations" in another mode. As a result, the Office Action fails to show that *Herrera* discloses, teaches, or suggests "dual mode sub-processing circuitry" that is operable to perform "motion compensation operations" associated with a two-dimensional image pipeline in one mode and to perform "rasterization operations" associated with a three-dimensional image pipeline in another mode.

For these reasons, the Office Action fails to establish that the proposed *DiNicola-Herrera* combination discloses, teaches, or suggests the Applicant's invention as recited in Claim 1 (and Claims 2-6 depending from Claim 1). For similar reasons, the Office Action fails to establish that the proposed *DiNicola-Herrera* combination discloses, teaches, or suggests the Applicant's invention as recited in Claims 7, 14, 20, and 26 (and Claims 8-13 depending from Claim 7, Claims 15-19 depending from Claim 14, and Claims 21-25 depending from Claim 20).

Accordingly, the Applicants respectfully request withdrawal of the §103(a) rejection and full allowance of Claims 1-26.

II. CONCLUSION

As a result of the foregoing, the Applicants assert that all pending claims are in condition for allowance and respectfully request an early allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Applicants have included the appropriate fee for a one (1) month extension of time. No additional fees are believed to be necessary. However, in the event that any additional fees are required for the prosecution of this application, please charge any necessary fees to Davis Munck, P.C. Deposit Account No. 50-0208.

Respectfully submitted,

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APPENDIX
PENDING CLAIMS

1. (Original) Image processing circuitry, comprising:

a two-dimensional image pipeline that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space;

a three-dimensional image pipeline that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable to perform motion compensation operations associated with said two-dimensional image pipeline in one mode and to perform rasterization operations associated said three-dimensional image pipeline in another mode.

2. (Original) The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to sample reference frames in said one mode and to perform texture mapping in said another mode.

3. (Original) The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said one mode and to blend samples from a plurality of texture maps in said another mode.

4. (Original) The image processing circuitry set forth in Claim 2 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error term in said one mode and to perform alpha blending in said another mode.

5. (Original) The image processing circuitry set forth in Claim 1 is operable to support at least one MPEG standard.

6. (Original) The image processing circuitry set forth in Claim 1 further comprising an alpha blend sub-circuitry that is operable to process at least 8- and 9-bit signed values.

7. (Original) For use in image processing circuitry that comprises a two-dimensional image pipeline and a three-dimensional image pipeline, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating dual mode sub-processing circuitry that is associated with both of said pipelines, said method comprising the steps of:

performing motion compensation operations associated with said two-dimensional image pipeline in one mode; and

performing rasterization operations associated said three-dimensional image pipeline in another mode.

8. (Original) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the steps of:

sampling reference frames in said one mode; and

performing texture mapping in said another mode.

9. (Original) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the step of blending one of samples from a plurality of reference frames in said one mode and samples from a plurality of texture maps in said another mode.

10. (Original) The method of operating said dual mode sub-processing circuitry set forth in Claim 8 further comprising the steps of:

processing said plurality of reference frames using error terms in said one mode; and

performing alpha blending in said another mode.

11. (Original) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the step of switching from said another mode to said one mode to perform motion compensation in accordance with at least one MPEG standard.

12. (Original) The method of operating said dual mode sub-processing circuitry set forth in Claim 10 wherein said performing alpha blending step further comprising the step of processing at least 8- and 9-bit signed values.

13. (Original) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the step of controlling said dual mode sub-processing circuitry.

14. (Original) Mode control circuitry for use in an image processing system having a two-dimensional image pipeline that processes two dimensional image data to generate successive two-dimensional image frames and a three-dimensional image pipeline that is operable to process three-dimensional image data to render successive three-dimensional image frames, said mode control circuitry comprising:

dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable to perform motion compensation operations associated with said two-dimensional image pipeline and to perform rasterization operations associated said three-dimensional image pipeline; and

a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in one mode and to perform said rasterization operations in said other mode.

15. (Original) The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to sample reference frames in said one mode and to perform texture mapping in said other mode.

16. (Original) The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said one mode and to blend samples from a plurality of texture maps in said other mode.

17. (Original) The mode control circuitry set forth in Claim 15 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error terms in said one mode and to perform alpha blending in said other mode.

18. (Original) The mode control circuitry set forth in Claim 14 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

19. (Original) The mode control circuitry set forth in Claim 14 further comprising an alpha blend sub-circuitry that is operable to process at least 8-bit and 9-bit signed values.

20. (Original) For use in image processing circuitry that comprises a two-dimensional image pipeline and a three-dimensional image pipeline, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating mode control circuitry that is associated with both of said pipelines, said method comprising the step of controlling dual mode sub-processing circuitry to at least one of perform motion compensation operations associated with said two-dimensional image pipeline in one mode, and perform rasterization operations associated said three-dimensional image pipeline in another mode.

21. (Original) The method of operating mode control circuitry set forth in Claim 20 further comprising the steps of:

sampling reference frames in said one mode; and

performing texture mapping in said other mode.

22. (Original) The method of operating mode control circuitry set forth in Claim 20 further comprising the steps of:

blending samples from a plurality of reference frames in said one mode; and

blending samples from a plurality of texture maps in said other mode.

23. (Original) The method of operating mode control circuitry set forth in Claim 21 further comprising the steps of:

processing said plurality of reference frames using error terms in said one mode; and

performing alpha blending in said other mode.

24. (Original) The method of operating mode control circuitry set forth in Claim 20 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

25. (Original) The method of operating mode control circuitry set forth in Claim 20 further comprising an alpha blend sub-circuitry that is operable to process at least 8-bit and 9-bit signed values.

26. (Original) A media processing system having a central processing unit, a memory subsystem, an image processing system, and a display system, said media processing system comprising:

a two-dimensional image pipeline that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of said display system;

a three-dimensional image pipeline that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable to perform motion compensation operations associated with said two-dimensional image pipeline in one mode and to perform rasterization operations associated said three-dimensional image pipeline in another mode.